Page 13 of 16

Appl. No. 10/572,612 Amendment and/or Response Reply to Office action of 3 October 2006

REMARKS/DISCUSSION OF ISSUES

By this Amendment, Applicant amends claims 1, 3, 5-8, and 11 and adds new claims 12-16. Claims 3 and 5 are rewritten in independent form without any change of scope. Claims 6, 7, 8 and 11 are amended to correct minor typographical errors, without any change of scope. New claims 12-14 are added to at least partially restore the original range of claims that existed before multiple dependencies were removed in the preliminary amendment. No new matter is added.

Accordingly, claims 1-16 are pending in the application.

The Examiner is respectfully requested to acknowledge the claim for priority and receipt of certified copies of all the priority documents. The Examiner is also respectfully requested to indicate whether or not the drawings are acceptable.

Applicant acknowledges the indication that claims 5-8 and 10-11 define patentable subject matter, and would be allowable if rewritten in independent form including all limitations of the base claim, and any intervening claims.

Reexamination and reconsideration are respectfully requested in view of the following Remarks.

35 U.S.C. § 102

The Office Action rejects claims 1-4 and 9 under 35 U.S.C. § 102 over <u>Kimura</u> WO200118962A1 ("<u>Kimura</u>").

Applicant respectfully submits that all of the claims 1-4 and 9 are patentable over Kimura for at least the following reasons.

Claim_1

Among other things, in the circuit of claim 1 the combining stage is arranged to convert differential input signals received by the differential signal input means into four gate signals respectively applied to the gate electrodes of the four transistors of the discriminating stage.

Applicant respectfully submits that it is apparent from inspection of FIG. 4 of <u>Kimura</u> that <u>Kimura</u> does not disclose such a feature.

. Atty. Docket No. FR030104

Appl. No. 10/572,612 Amendment and/or Response Reply to Office action of 3 October 2006 Page 14 of 16

Accordingly, for at least this reason, Applicant respectfully submits that claim 1 is patentable over Kimura.

Claims 2, 4 and 9

Claim 2, 4 and 9 depend from claim 1 and are deemed patentable over <u>Kimura</u> for at least the reasons set forth above with respect to claim 1.

Claim 3

Claim 3 has been rewritten in independent form.

Among other things, in the circuit of claim 3 the gate signals applied to the respective gate electrodes of the four transistors of the discriminating stage are tristate voltage signals so designed that a single one of said gate electrodes, selected from the differential input signals received by the differential signal input means, has a maximum or minimum voltage value.

Applicant respectfully submits that <u>Kimura</u> does not disclose such a combination of features.

The Office action cites the signals QP and QN as two of the signals applied to the respective gate electrodes of the four transistors of the discriminating stage, which is alleged to comprise transistors B5-B8.

However, inspection of FIG. 3 of <u>Kimura</u> clearly shows that the signals QP and QN are each only bi-level signals, and not tri-state voltage signals as recited in claim 3. Furthermore, FIG. 3 also shows that the signals OIP and OIN are four-state voltage signals, not tri-state voltage signals.

Therefore, FIG. 4 of Kimura cannot disclose the electronic circuit of claim 3.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 3 is patentable over Kimura.

NEW CLAIMS 12-16

New claims 12-14 depend from claim 3, and new claims 15-16 depend from claim 1, and are deemed patentable for at least the reasons set forth above with respect to claims 1 and 3, respectively, and for the following additional reasons.

Atty. Docket No. FR030104

Page 15 of 16

Appl. No. 10/572,612 Amendment and/or Response Reply to Office action of 3 October 2006

Claim 14

Among other things, claim 14 recites the same features as recited in claim 5, which has already been indicated by the Examiner to define patentable subject matter.

Claim 15

Among other things, in the electronic circuit of claim 15, the combining stage is adapted to receive a first differential input signal pair a and aq and a second differential input signal pair b and bq.

The Office Action states that transistors B1-B4 in FIG. 4 of <u>Kimura</u> supposedly correspond to the combining stage. However, the transistors B1 and B4 receive only a single differential input signal pair DP and DN, while the transistors B2 and B3 do not receive any second differential input signal pair, but instead receive signals from transistors B9 and B10 both of which are driven by the same signal CN (CP is not provided to transistors B1-B4).

Accordingly, for at least this additional reason, claim 15 is deemed patentable over Kimura.

Claim 16

Among other things, in the electronic circuit of claim 16, the combining stage is adapted to convert the first and second differential input signal pairs into the four gate signals as (a + b), (a + bq), (bq + a) and (aq + bq), respectively, to be applied to the gate electrodes of the four transistors of the discriminating stage.

No such feature is disclosed by <u>Kimura</u>. For example, the Office Action states that the four transistors of the discriminating stage correspond to transistors B5-B8 of FIG. 4 of <u>Kimura</u>. However, the gate electrodes of the transistors B5-B8 do not receive four gate signals as (a + b), (a + bq), (bq + a) and (aq + bq). In particular, transistors B6 and B7 receive signals from transistors B11 and B12 both of which are driven by the same signal CP.

Accordingly, for at least these additional reasons, claim 16 is deemed patentable over Kimura.

Atty. Docket No. FR030104

Appl. No. 10/572,612 Amendment and/or Response Reply to Office action of 3 October 2006 Page 16 of 16

REQUEST FOR ENGLISH TRANSLATION OF CITED DOCUMENT

In the event that this application is not allowed and any rejections are maintained based in whole or in part upon <u>Kimura</u>, pursuant to MPEP 706.02 Applicant respectfully requests that the Examiner provide an English translation of Kimura.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1-16 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment (except for the issue fee) to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.

Date: 29 December 2006

By: Kenneth D. Springer

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Atty. Docket No. FR030104